

ED5-3-INV

Scalable packaging and wiring for superconducting quantum computers

*Shuhei Tamate¹

Research Center for Advanced Science and Technology (RCAST), University of Tokyo¹

Superconducting qubit devices are one of the promising candidates for realizing large-scale quantum computer. The next challenge toward building quantum computer would be implementation of quantum error correction. To implement realistic quantum error correction codes, such as surface codes, we need to prepare two-dimensional array of superconducting qubits in a scalable way. It naturally requires three-dimensional wiring to superconducting qubits, which suppose to have at least one microwave control line for every qubit. A lot of efforts have been made recently to establish three-dimensional wiring techniques which ensure scalability of superconducting qubit devices. The techniques include flip-chip bonding [1], through-silicon vias [2], contact probes [3], and direct coaxial cable wiring [4].

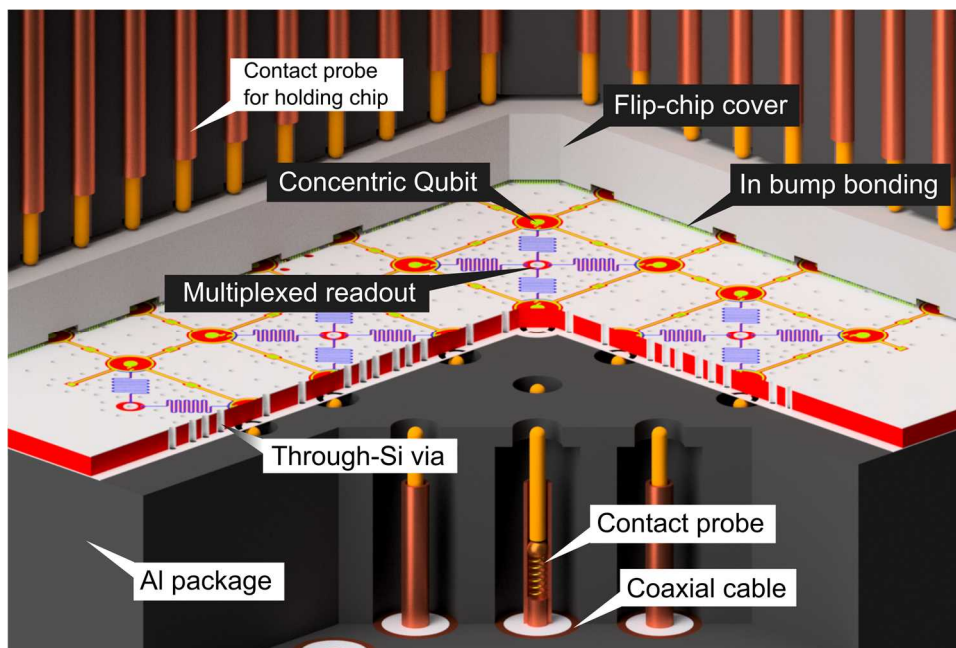
In this talk, we present a way to realize scalable packaging and wiring for superconducting qubits by using direct vertical interconnect between superconducting circuits and coaxial cables. The design of our package is shown in Fig. 1. In our package, coaxial cables for qubit control and readout are directly wired from the bottom of the superconducting qubit chip. The electrical contact between superconducting circuits and coaxial cables are provided by contact probes. The electromagnetic fields from the cables are guided by through-silicon vias and transmitted to the superconducting circuits on top of the chip. This wiring scheme is fully vertical and two-dimensionally scalable. We report the results of characterization of the package and measurements of the multi-qubit chip in this package.

[1] B. Foxen et al., *Quantum Science and Technology* 3, 014005 (2018).

[2] D. Rosenberg et al., *npj Quantum Information* 3, 42 (2017).

[3] N. T. Bronn et al., *Quantum Science and Technology* 3, 024007 (2018).

[4] J. Rahamim et al., *Appl. Phys. Lett.* 110, 222602 (2017).



Keywords: Quantum computing, Scalable qubit packaging, Vertical interconnects