EDP1-4

Implementation of interface circuit for Digital SQUID with sub-Flux Quantum Feedback Resolution

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Digital SQUIDs with the single flux quantum (SFQ) feedback have attracted much attention because of the feasibility of realizing a wide dynamic range and high slew rate for digital magnetometers. In order to realize higher resolution, we have studied a digital SQUID with sub-flux quantum feedback. In this presentation, we will discuss implementation methods for an interface circuit considering circuit size, power consumption and signal processing in order to realize high-resolution and high-speed operation of the digital SQUID magnetometer. Assuming the decimation filter and the up/down counter implemented on a FPGA board, a 1-bit to 16-bit deserializer with output frequency of 500 MHz can be used for interface circuit. This would drastically reduce bias current for the digital SQUID with SFQ feedback operating at 4.2 K.

Acknowledgement

This study has been partially supported by the VLSI Design and Education Center (VDEC) at the University of Tokyo, in collaboration with Cadence Design Systems, Inc. Circuits were fabricated in the clean room for analog-digital superconductivity (CRAVITY) of the National Institute of Advanced Industrial Science and Technology (AIST) with the standard process 2 (STP2) and the high-Jc standard process (HSTP). The AIST-STP2 and HSTP process are based on the Nb circuit fabrication process developed by the International Superconductivity Technology Center (ISTEC).

Keywords: digital SQUID, Single flux quantum (SFQ) circuit, sub-SFQ feedback, digital filter