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Single-Flux-Quantum Parallel Multiplier Using Accumulator Unit

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A multiplier is one of fundamental circuit elements for digital circuits. So far, single-flux-quantum (SFQ) multipliers based on various hardware algorithms have been investigated. Conventional SFQ multipliers required relatively large circuit areas because the adder tree is used to sum partial products. In this study, we investigated and designed a new SFQ parallel multiplier that uses a parallel accumulator unit. Because the accumulator unit, which is composed of resettable toggle flip-flops, can be used as the parallel counter, the circuit area for summation of partial products can be drastically reduced. We designed and simulated a 4-bit SFQ parallel multiplier based on the investigated hardware algorithm using the AIST 10 kA/cm^2 Nb advanced process. The target operating frequency is 30 GHz. The multiplier can be used as a multiplier-accumulator (MAC). Thought the operating frequency of the designed multiplier is slightly lower than that of the conventional SFQ parallel multiplier, the circuit area can be reduced. The number of Josephson junction to implement 4-bit multiplier is 1374, which is approximately half of that of the conventional 4-bit SFQ parallel multiplier.

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