EDP2-3

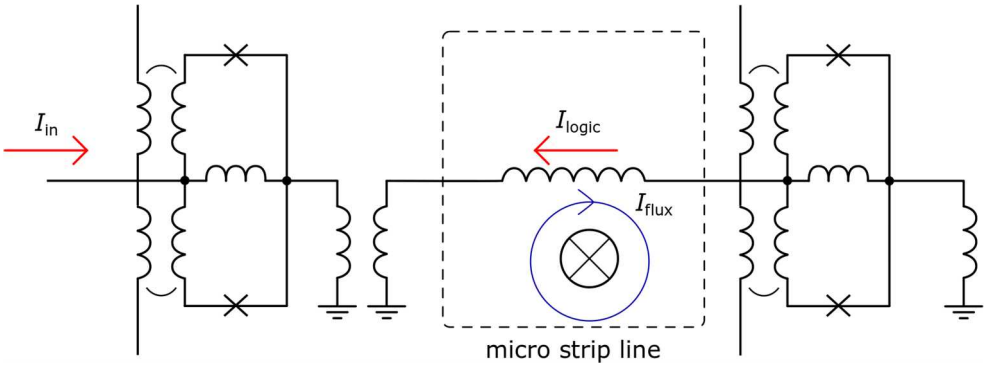
Investigation of influence by flux trapping for interconnection of adiabatic quantum-flux-parametron circuits

*Tomoyuki Tanaka[1], Christopher L. Ayala[2], Nobuyuki Yoshikawa[1,2]

Graduate School of Engineering Science, Yokohama National University[1]
Institute of Advanced Sciences, Yokohama National University[2]

Adiabatic quantum-flux-parametron (AQFP) logic is known as an energy efficient superconductor digital logic family [1]. When compared to the state-of the-art CMOS technology, AQFP has a high advantage in term of power consumption. To realize large scale AQFP integrated circuit, many studies are ongoing [2][3].
One problem that has recently emerged is low yield of circuits with complex interconnect. One possible cause is magnetic flux trapping. A trapped magnetic flux is a physical phenomenon that occurs mainly in the ground layer. When a normal conduction region is surrounded by a superconducting one, permanent current flows around that region. The current and magnetic flux are thought to affect the circuit and cause malfunctions.
The logic state of an AQFP circuit is encoded as the direction of current, and each AQFP gate are connected by a superconducting stripline. The amplitude of the data signal current maybe smaller than the circular current that is generated by the trapped flux, especially for long, complex interconnect whose large parasitic inductance already attenuates the AQFP current output. Therefore, circuit malfunctions may happen as the data current signal is negatively influenced by trapped flux along the interconnect, resulting in the incorrect sampling of data in the receiving AQFP gate.
It is very difficult to completely avoid magnetic flux trapping. One solution is adapting moats along the interconnection. Moats are done by creating slits in the ground plane, and by creating defects such that trapped flux are guided to the moat [4]. In this time, we designed a test circuit with the application of various moat structures and considered its effectiveness in AQFP circuits.

[1] Takeuchi, N., Ehara, K., Inoue, K., Yamanashi, Y., & Yoshikawa, N., IEEE Transactions on Applied Superconductivity, 23(3), 1700304–1700304 (2013).
[2] Yamae, T., Takeuchi, N. & Yoshikawa, N., Supercond. Sci. Technol. 32, 035005 (2019).
[3] Cai, R. et al., in Proceedings of the 46th International Symposium on Computer Architecture 567–578 (ACM, 2019).
[4] Polyakov, Y., Narayana, S. & Semenov, V. K., IEEE Trans. Appl. Supercond. 17, 520–525 (2007).



Keywords: Superconducting integrated circuit, Adiabatic Quantum Flux Prametron, Flux Trapping