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Adiabatic Quantum-Flux-Parametron Design-For-Testability Components for Large-Scale Digital Circuits

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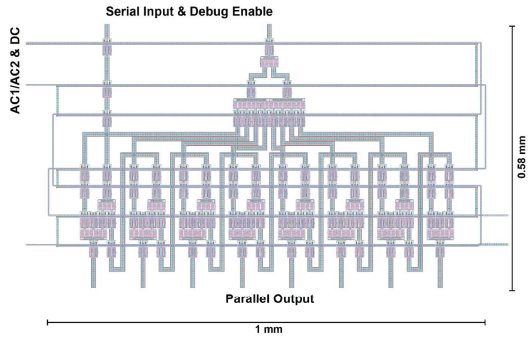
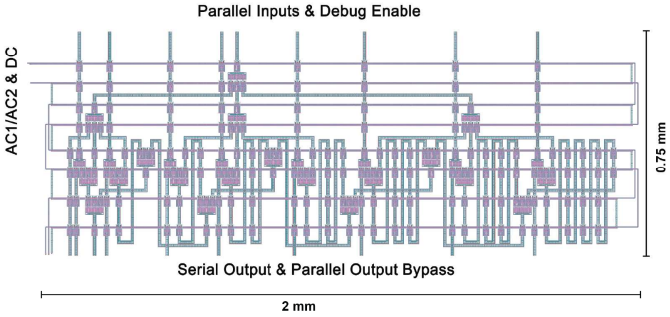
Adiabatic quantum-flux-parametron (AQFP) logic can operate with bit energies below $50k_BT$ at a clock frequency of 5 GHz, which makes it a suitable foundation for building energy-efficient computing systems. Complex circuits such as a microprocessor would benefit from additional circuitry to facilitate prototype testing during experimental measurement. Thus, we developed design-for-testability (DFT) components for use in the testing of an AQFP microprocessor, namely parallel-to-serial (P2S) and serial-to-parallel (S2P) data converters. These DFT components allow one to probe between processor sub-units while reducing the area overhead of I/O pads and off-chip interfaces typically needed to read-out intermediate signals. Because of the free-running, non-gated clock needed for AQFP, their design differs than that of their SFQ variants which have separate load and read control clocks. Instead, the AQFP variants use a debug control signal to isolate data of interest (in P2S) or block subsequent dataflow (in S2P) from interfering with the serialization/parallelization process. We developed 8-bit AQFP P2S/S2P units (~400 Josephson junctions and 1 mm^2 area each) and demonstrated fully correct operation.



Serial-to-Parallel Data Converter



Parallel-to-Serial Data Converter

Keywords: aqfp, design-for-testability, digital, microprocessor